ART FILM - detail1

NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:
   A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES 600-60612-01_02.ZIP
   B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.
   C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.
   D. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381 [.015] MAX RADIUS.
   E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.
   F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2. DIELECTRIC MATERIAL:
   A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (RoHS COMPLIANT EPOXY-GLASS).
   B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF.076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.
   C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.
   D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

3. DRILLING:
   A. VIA DIAMETERS (TOL. = +.051/- DRILL DIAMETER [+.0020/- DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.
   B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.
   C. FILL ALL THRU VIAS USING NON-CONDUCTIVE EPOXY AND OVERPLATE WITH COPPER, .005 [.0002] MINIMUM THICKNESS. DIMPLE DEPTH IN BGA PADS SHALL BE .025 [.001] MAXIMUM. THE PRESENCE OF WRAP PLATING SHALL BE VISUALLY EVIDENT IN ALL QUALITY CONFORMANCE MICROSECTIONS; NO MINIMUM MEASUREMENT REQUIRED.

4. SOLDER MASK:
   A. APPLY LPI SOLDER MASK USING PROVIDED DATA.
   B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR BLUE.
   C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

5. MARKING:
   A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

6. ELECTRICAL TEST:
   A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.
   B. ALL PCBS SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.
   C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.

7. FINAL FINISH:
   A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSION GOLD (ENIG) PER IPC-4552.

8. IMPEDANCE:
   A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.
   B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.

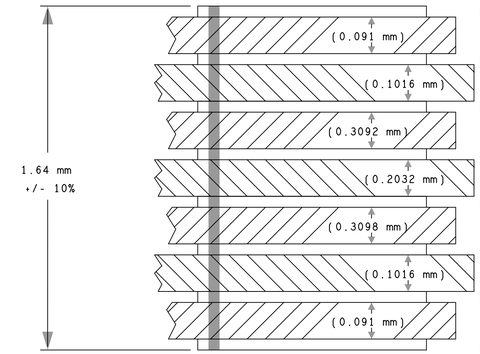
9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBS SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.

10. ENSURE ALL THE VIA HOLES ARE FILLED WITH SOLDER MASK TO ENSURE GOOD QUALITY OF SILK SCREEN PRINT.

11. SILKSCREEN SHALL BE PERMANENT NON-CONDUCTIVE INK AND WITH NO OVERLAP ON ANY COMPONENT PAD OR THROUGH HOLE.EXCESS SILK OVERLAPPING ON PADS CAN BE TRIMMED.

12. VIA ON PAD TO BE TAKEN CARE WITH CAP PLATING & CAN BE FILLED BY TYPE VII OR TYPE VI as per Fabrication Ability.

STACK-UP



LAYER DESCRIPTION	START COPPER WT	SE IMP OHMS	SE TRACE WIDTH	REF LAYER	CPW SPACE	DIFF IMP OHMS	DIFF TRACE WIDTH/SPACE	REF LAYER	CPW SPACE
L01 - TOP	1.0 OZ	50E	0.1143 mm	02	------	90E 100E	0.1237/0.1557 mm 0.1078/0.2097 mm	02	------
L02 - PLANE	1.0 OZ	--	-----	---	------	---	----	---	------
L03 - SIGNAL	1.0 OZ	50E	0.1097 mm	02	------	90E 100E	0.1127/0.1667 mm 0.0944/0.2104 mm	02	------
L04 - PLANE	1.0 OZ	--	.-----	---	------	---	.-----/.-----	---	------
L05 - PLANE	1.0 OZ	--	.-----	---	------	---	.-----/.-----	---	------
L06 - SIGNAL	1.0 OZ	50E	0.1097 mm	07	------	90E 100E	0.1127/0.1667 mm 0.0944/0.2104 mm	07	------
L07 - PLANE	1.0 OZ	--	-----	---	------	---	----	---	------
L08 - BOTTOM	1.0 OZ	50E	0.1143 mm	07	------	90E 100E	0.1237/0.1557 mm 0.1078/0.2097 mm	07	------

NOTE: PREPERG THICKNESS BETWEEN POWER TO SIGNAL LAYERS MUST BE TWICE OR MORE THAN TWICE OF PREPERG THICKNESS BETWEEN SIGNAL TO GROUND LAYERS.

SEE BOM	SEE BOM
NEXT ASSY	USED ON
APPLICATION	

THE INFORMATION CONTAINED HEREIN IS CONFIDENTIAL AND PROPRIETARY TO CYPRESS SEMICONDUCTOR AND SHALL NOT BE REPRODUCED OR DISCLOSED IN WHOLE OR IN PART OR USED FOR ANY DESIGN, MANUFACTURE, OR OTHERWISE, EXCEPT WHEN SUCH USER POSSESSES AUTHORIZATION FROM CYPRESS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN METRIC WITH INCHES IN BRACKETS
.XXX ±.064 [±.005] .XX ±.13 [±.01] ANGLES ±.5°

MATERIAL 2

FINISH 7

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN HUSA	21/07/22
ENGINEER MISHRASANATK	21/07/22
CHECKER -	-
QA -	-
PROJ. ENG. -	-

198 CHAMPION COURT
SAN JOSE, CA 95134
(408) 943-2600

TITLE PCB FABRICATION,

FX3_USB3_VISION_SOLUTION_DEMO

SIZE	CAGE CODE	CY P/N
D	-	610-60624-01

SCALE	SHEET	REV
""	1 OF 2	01

COMPUTER GENERATED DRAWING
DO NOT CHANGE MANUALLY

ALLEGRO FILE: 600-XXXXX-XX_02.BRD

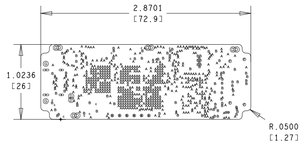
FAB NOTES REV 04/05/17

ART FILM - detail1

DRILL CHART: TOP TO BOTTOM

	ALL UNITS ARE IN MILLIMETER			
FIGURE	FINISHED SIZE	TOLERANCE (+/-)	PLATED	QTY
A	0.2032	+0.0762/-0.0762	PLATED	714
B	0.254	+0.0762/-0.0762	PLATED	83
H	0.3	+0.5/-0.3	PLATED	2
+	0.3048	+0.0762/-0.0762	PLATED	11
G	0.71	+0.0762/-0.0762	PLATED	10
B	1.1	+0.0762/-0.0762	PLATED	4
D	1.5	+0.0762/-0.0762	PLATED	4
G	1.9	+0.0508/-0.0508	NON-PLATED	2
OD	1.4x0.4	+0.0508/-0.0508	PLATED	2
OD	2.1x0.4	+0.0508/-0.0508	PLATED	2

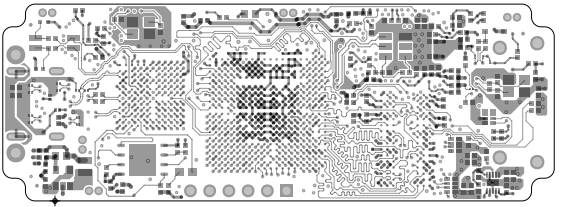
TOTAL HOLES: 836



THE INFORMATION CONTAINED HEREIN IS CONFIDENTIAL AND PROPRIETARY TO CYPRESS SEMICONDUCTOR AND SHALL NOT BE REPRODUCED OR DISCLOSED IN WHOLE OR IN PART OR USED FOR ANY DESIGN, MANUFACTURE, OR OTHERWISE, EXCEPT WHEN SUCH USER POSSESSES DIRECT, WRITTEN AUTHORIZATION.	SIZE D	CAGE CODE -	CY P/N 610-60624-01
	SCALE NTS		SHEET 2 OF 2 / REV 01
	COMPUTER GENERATED DRAWING DO NOT CHANGE MANUALLY		

ALLEGRO FILE: 600-XXXXX-XX_02.BRD

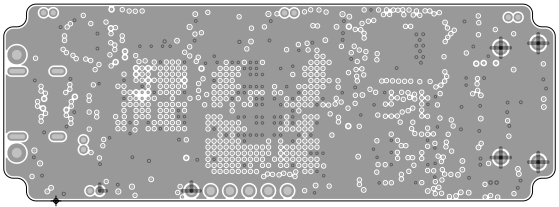
ART FILM - 01_TOP



SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY-RB4111 FX3_USB3_VISION_SOLUTION_DEMO		
	DRAWN BY:HUSA		
	LAYER:TOP SIDE		
	DWG NO: 600-60624-01	REV:01	DATE:21/07/22

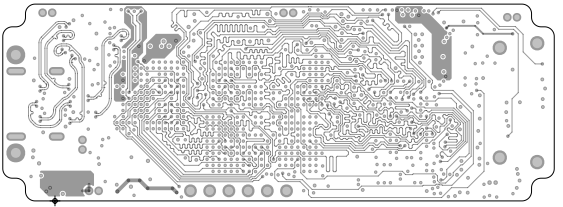
ART FILM - 01_TOP

ART FILM - 02_GND1

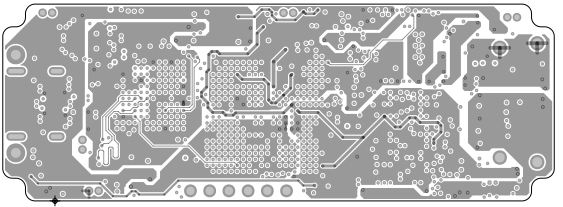


SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY-RB4111 FX3_USB3_VISION_SOLUTION_DEMO		
	DRAWN BY:HUSA		
	LAYER:02_GND1		
	DWG NO: 600-60624-01	REV:01	DATE:21/07/22

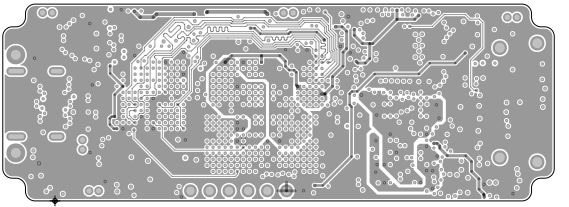
ART FILM - 02_GND1



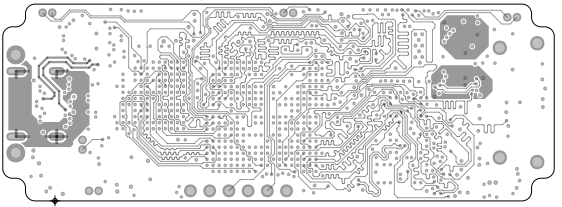
SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY-RB4111 FX3_USB3_VISION_SOLUTION_DEMO		
	DRAWN BY:HUSA		
	LAYER:03_SIG1		
	DWG NO: 600-60624-01	REV:01	DATE:21/07/22



SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY-RB4111 FX3_USB3_VISION_SOLUTION_DEMO		
	DRAWN BY:HUSA		
	LAYER:04_PWR1		
	DWG NO: 600-60624-01	REV:01	DATE:21/07/22

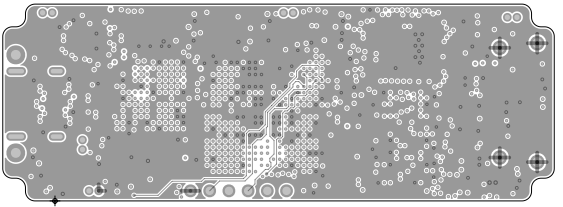


SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY-RB4111 FX3_USB3_VISION_SOLUTION_DEMO		
	DRAWN BY:HUSA		
	LAYER:05_PWR2		
	DWG NO: 600-60624-01	REV:01	DATE:21/07/22



SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY-RB4111 FX3_USB3_VISION_SOLUTION_DEMO		
	DRAWN BY:HUSA		
	LAYER:06_SIG1		
	DWG NO: 600-60624-01	REV:01	DATE:21/07/22

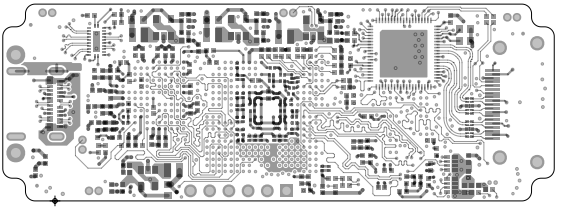
ART FILM - 07_GND2



SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY-RB4111 FX3_USB3_VISION_SOLUTION_DEMO		
	DRAWN BY:HUSA		
	LAYER:07_GND2		
	DWG NO: 600-60624-01	REV:01	DATE:21/07/22

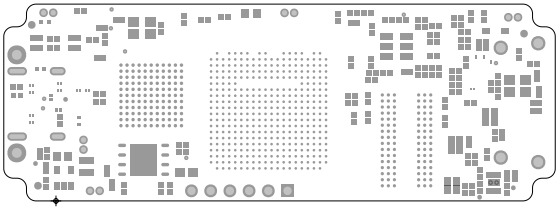
ART FILM - 07_GND2

ART FILM - 08_BOTTOM



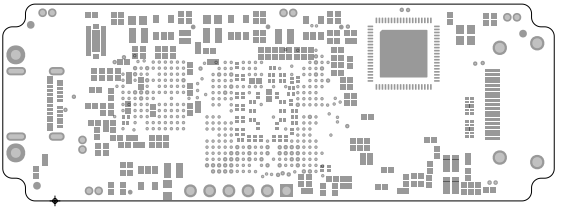
SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY-RB4111 FX3_USB3_VISION_SOLUTION_DEMO		
	DRAWN BY:HUSA		
	LAYER:SIDE MOTTOB		
	DWG NO: 600-60624-01	REV:01	DATE:21/07/22

ART FILM - 08_BOTTOM



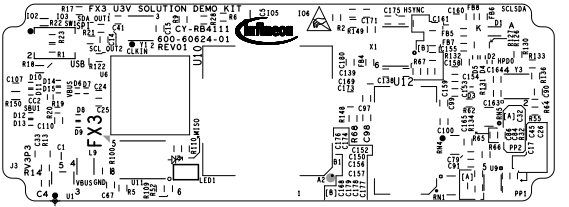
SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY-RB4111 FX3_USB3_VISION_SOLUTION_DEMO		
	DRAWN BY:HUSA		
	LAYER:SOLDERMASK TOP		
	DWG NO: 600-60624-01	REV:01	DATE:21/07/22

ART FILM - smb

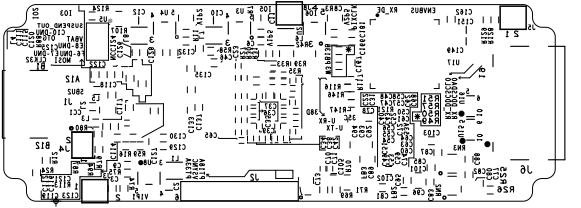


SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY-RB4111 FX3_USB3_VISION_SOLUTION_DEMO		
	DRAWN BY:HUSA		
	LAYER:SOLDERMASK BOTTOM		
	DWG NO: 600-60624-01	REV:01	DATE:21/07/22

ART FILM - smb



Infineon SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY-RB4111 FX3_USB3_VISION_SOLUTION_DEMO		
	DRAWN BY:HUSA		
	LAYER:SILKSCREEN TOP		
	DWG NO: 600-60624-01	REV:01	DATE:21/07/22



Infineon SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY-RB4111 FX3_USB3_VISION_SOLUTION_DEMO		
	DRAWN BY:HUSA		
	LAYER:BOTTOM SILKSCREEN		
	DWG NO: 600-60624-01	REV:01	DATE:21/07/22

SX3 HDMI 4K CAPTURE DONGLE RDK
SINGLE DIMENSION - 72.9 X 26 MM
PANEL DIMENSION - 162.97 X 125.95 MM
ROUTING TOLERANCE-(+/-)0.2MM

